ACE25AC16S

SPI Serial EEPROM

Description

The ACE25AC16S is 16,384 bits of serial Electrical Erasable and Programmable Read Only Memory, commonly known as EEPROM. They are organized as 2048 words of 8 bits (one byte) each. The devices are fabricated with proprietary advanced CMOS process for low power and low voltage applications. These devices are available in standard 8-lead DIP, 8-lead SOP, 8-lead TSSOP packages. The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The $\overline{\text{HOLD}}$ pin may be used to suspend any serial communication without resetting the serial sequence. While the device is paused, transitions on its inputs will be ignored. Our extended V_{CC} range (1.8V to 5.5V) devices enables wide spectrum of applications.

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- Data Sheet Describes Mode 0 Operation
- Low voltage and low power operations
- ACE25AC16S: VCC = 1.8V to 5.5V
- 20MHz clock rate (5V)
- Maximum Standby current < 1μA (typically 0.02μA and 0.06μA @ 1.8V and 5.5V respectively).
- Partial page write operation allowed (32 bytes page write mode).
- Self-timed programming cycle (5 ms max).
- Block Write Protection (Protect 1/4, 1/2, or Entire Array).
- Write protect pin for hardware data protection.
- High reliability: typically 1,000,000 cycles endurance.
- 100 years data retention.
- Industrial temperature range (-40℃to 85℃).
- Standard 8-pin DIP/SOP/TSSOP Pb-free packages.

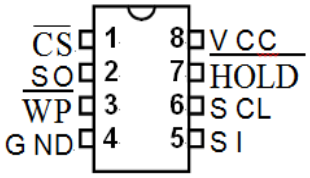
Absolute Maximum Ratings

Industrial operating temperature:	-40℃ to 85℃
Storage temperature:	-50℃ to 125℃
Input voltage on any pin relative to ground:	-0.3V to V_{CC} + 0.3V
Maximum voltage:	8V
ESD Protection on all pins:	>2000V

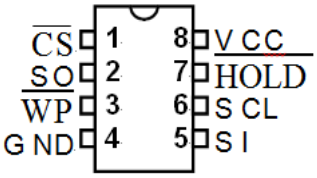
Notice: Stresses exceed those listed under “Absolute Maximum Rating” may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality.

Packaging Type

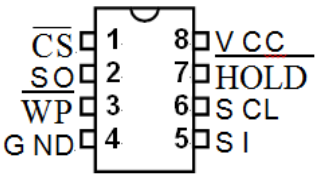
DIP-8



SOP-8



TSSOP-8



Pin Configurations

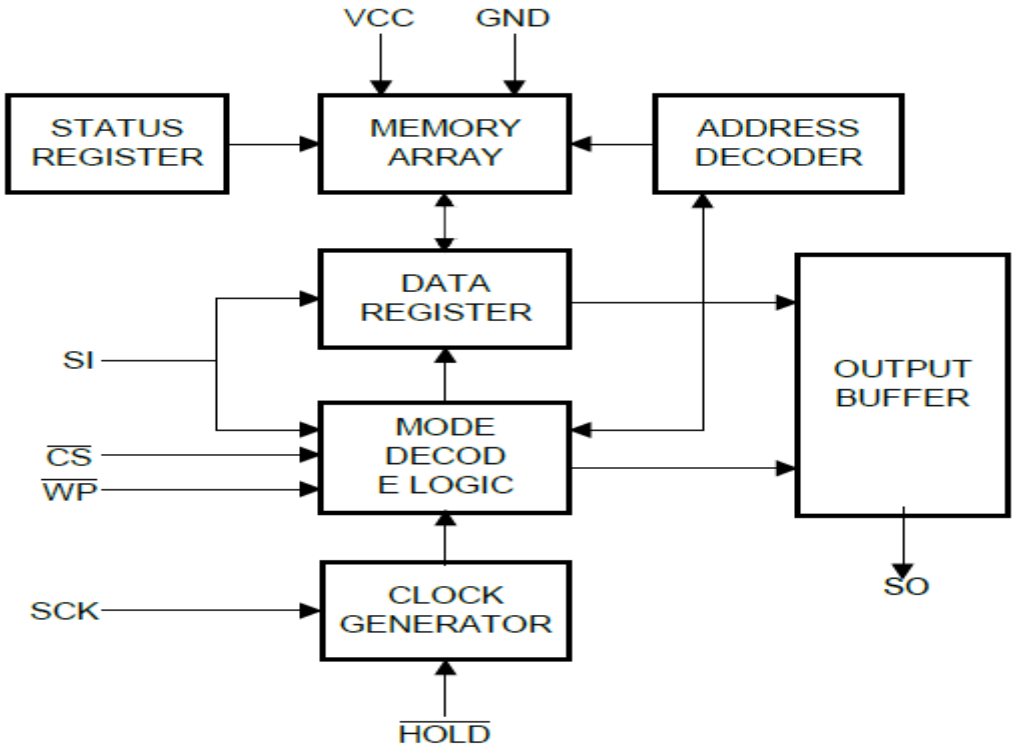
Pin Name	Functions
$\overline{CS}$	Chip Select
SCL	Serial Clock Input
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protest
$\overline{HOLD}$	Suspends Serial Input

Ordering information

ACE25AC16S XX + X H

- Halogen-free
- U: Tube
  T: Tape and Reel
- Pb - free
- DP: DIP-8
  FM: SOP-8
  TM: TSSOP-8

Block Diagram



Pin Descriptions

(A) CHIP SELECT ($\overline{CS}$)

The ACE25AC16S is selected when the $\overline{CS}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

(B) Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses, and data. Data is latched on the rising edge of the serial clock.

(C) Serial Output (SO)

The SO pin is used to transfer data out of the ACE25AC16S. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

(D) Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the ACE25AC16S. Instructions, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

(E) Write Protect ($\overline{WP}$)

This pin is used in conjunction with the WPEN bit in the status register to prohibit writes to the non-volatile bits in the status register. When $\overline{WP}$ is low and WPEN is high, writing to the non-volatile bits in the status register is disabled. All other operations function normally. When $\overline{WP}$ is high, all functions, including writes to the non-volatile bits in the status register operate normally. If the WPEN bit is set, $\overline{WP}$ low during a status register write sequence will disable writing to the status register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write. The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is low. This allows the user to install the ACE25AC16S in a system with $\overline{WP}$ pin grounded and still be able to write to the status register. The $\overline{WP}$ pin functions will be enabled when he WPEN bit is set high.

(F) Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ pin to select the ACE25AC32S. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ can be used to pause the serial communication with, the master device without resetting the serial sequence. To pause, the $\overline{HOLD}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{HOLD}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{HOLD}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

Memory Organization

The ACE25AC16S devices have 64 pages respectively. Since each page has 32 bytes, random word addressing to ACE25AC16S will require 11 bits data word addresses respectively.

Device Operation

The ACE25AC16S utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table A. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low $\overline{CS}$ transition.

Table A. Instruction Set for the ACE25AC16S

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Memory Array
WRITE	0000 X010	Write Data to Memory Array

Status Register Operation

Table B. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Write Enable (WREN)

The device will power up in the write disable state when VCC is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

Write Disable (WRDI)

To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{WP}$ pin.

Read Status Register (RDSR)

The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the block write protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table C. Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{RDY}$)	Bit 0 = “0” ($\overline{RDY}$) indicates the device is READY. Bit 0 = “1” indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1= “0” indicates the device is not WRITE ENABLED. Bit 1 = “1” indicates the device is write enabled.
Bit 2 (BP0)	See table D.
Bit 3 (BP1)	See table D.
Bits 4-6 are “0”s when device is not in an internal write cycle.	
Bit 7 (WPEN)	See table E.
Bits 0-7 are “1” during an internal write cycle.	

Write Status Register (WRSR)

The WRSR instruction allows the user to select one of four levels of protection. The ACE25AC16S is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read only. The block write protection levels and corresponding status register control bits are shown in Table D. The three bits BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells.

Table D. Block Write Protect Bits

Level	Status Register Bit		Array Address Protected
	BP1	BP0	
0	0	0	None
1(1/4)	0	1	0600-07FF
2(1/2)	1	0	0400-07FF
3(All)	1	1	0000-07FF

The WRSR instruction also allows the user to enable or disable the write protect ($\overline{WP}$) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is “1”. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is “0”. When the device is hardware write protected, writes to the status register, including the block protect bits and the WPEN bit, and the block-protected sections in the memory array are disabled. Writes are only allowed to sections of the memory that are not block-protected.

NOTE: When the WPEN bit is hardware write protected, it cannot be changed back to “0” as long as the $\overline{WP}$ pin is held low.

Table E. Wpen Operation

WPEN	WP	WEN	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writeable	Writeable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writeable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writeable	Writeable

EEPROM Operation

Read Data Bytes (READ)

Reading the ACE25AC16S via the serial output (SO) pin requires the following sequence. After the $\overline{CS}$ line is pulled low to select a device, the read op-code is transmitted via the SI line followed by the byte address to be read (A15−A0, see Table F). Upon completion, any data on the SI line will be ignored. The data (D7−D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address (0000h), allowing the entire memory to be read in one continuous read cycle.

Write Sequence (WRITE)

In order to program the ACE25AC16S, two separate instructions must be executed. First, the device must be write enabled via the WREN instruction. Then a Write (WRITE) instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code is transmitted via the SI line followed by the byte address (A15−A0) and the data (D7–D0) to be programmed (See Table F). Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.

The ACE25AC16S is capable of a 32-byte page write operation. After each byte of data is received, the five low-order address bits are internally incremented by one; the high order bits of the address will remain constant. If more than 32 bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The ACE25AC16S is automatically returned to the write disable state at the completion of a write cycle.

NOTE: If the device is not write enabled (WREN), the device will ignore the write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to reinitiate the serial communication.

The READY/BUSY status of the device can be determined by initiating a read status register (RDSR) instruction. If Bit 0 = “1”, the write cycle is still in progress. If Bit 0 = “0”, the write cycle has ended. Only the RDSR instruction is enabled during the write programming cycle.

Table F. Address Key

Address	ACE25AC16S
A_N	A_{10}-A_0
Don't Care Bits	A_{15}-A_{11}

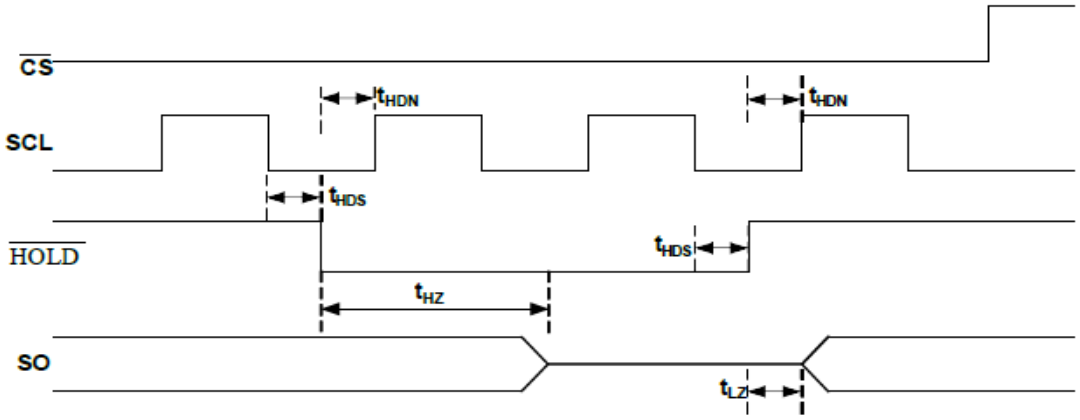


Figure 1: HOLD Timing

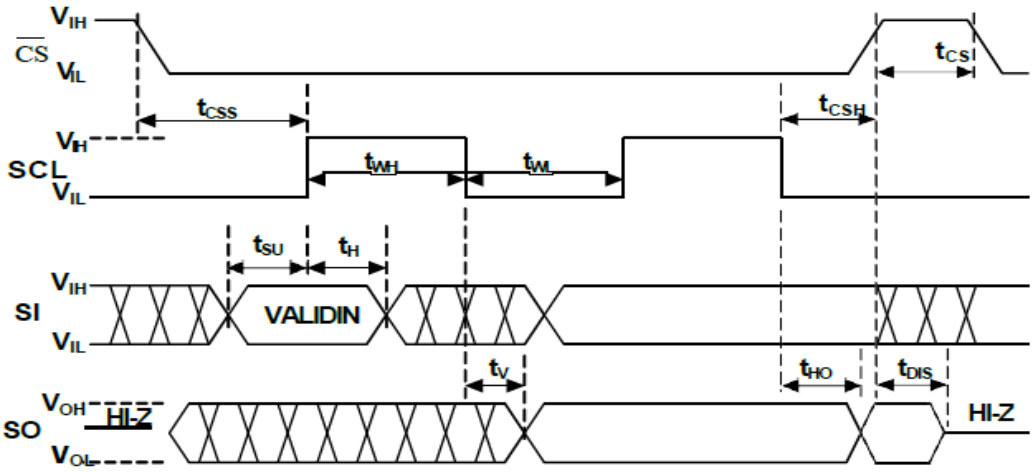


Figure 2: Synchronous Date Timing(for Mode 0)

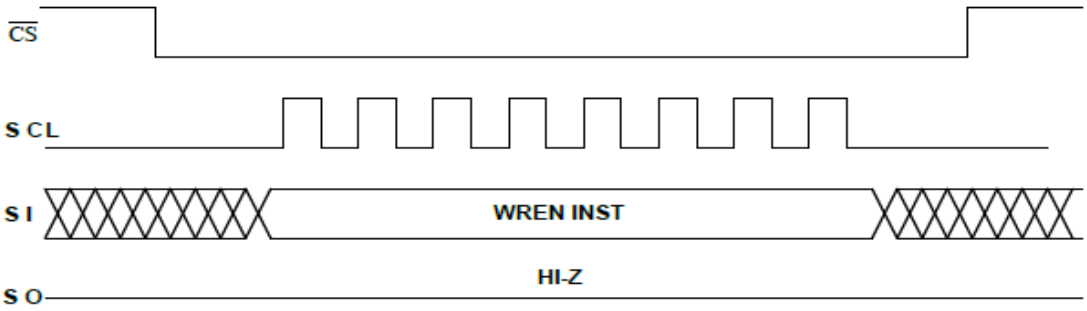


Figure 3: WREN Timing

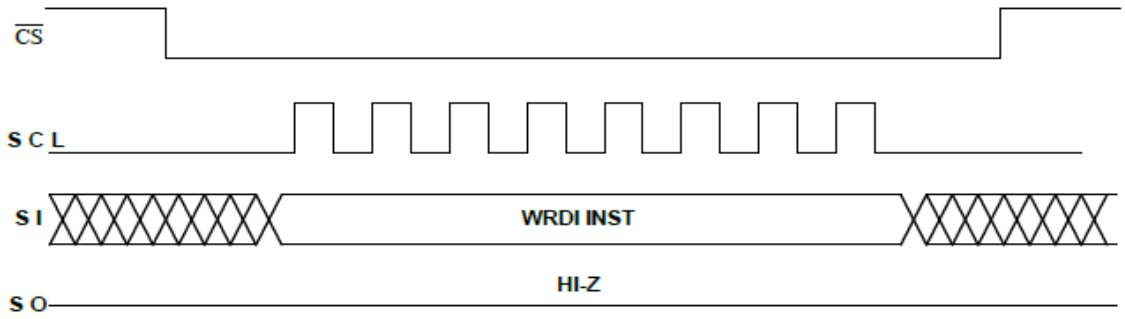


Figure 4: WRDI Timing

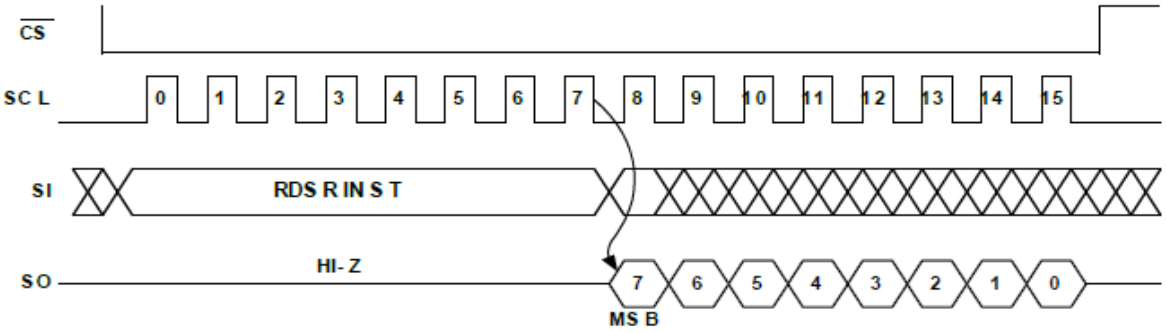


Figure 5: RDSR Timing

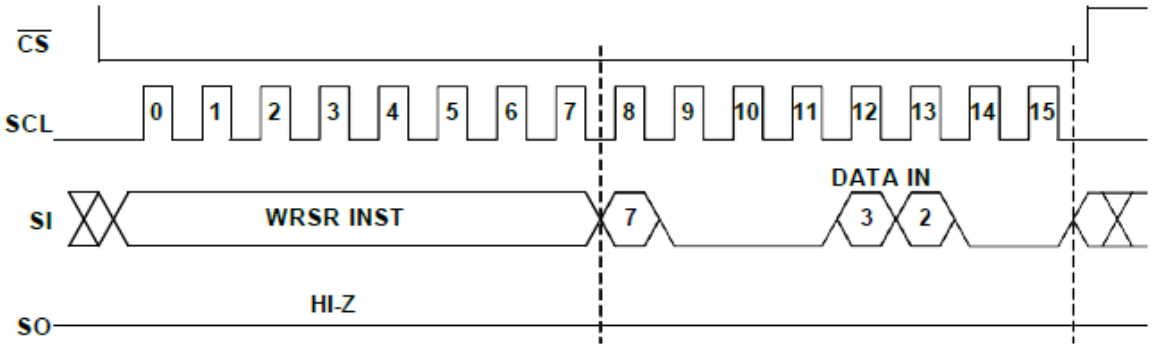


Figure 6: WRSR Timing

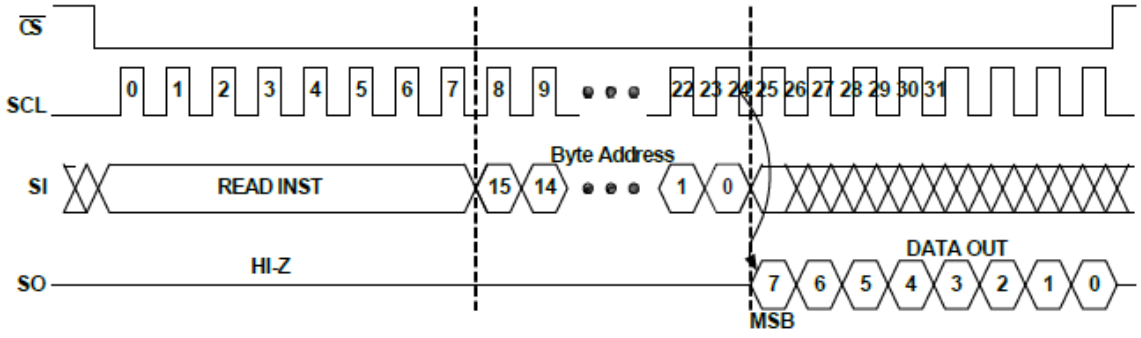


Figure 7: READ Timing

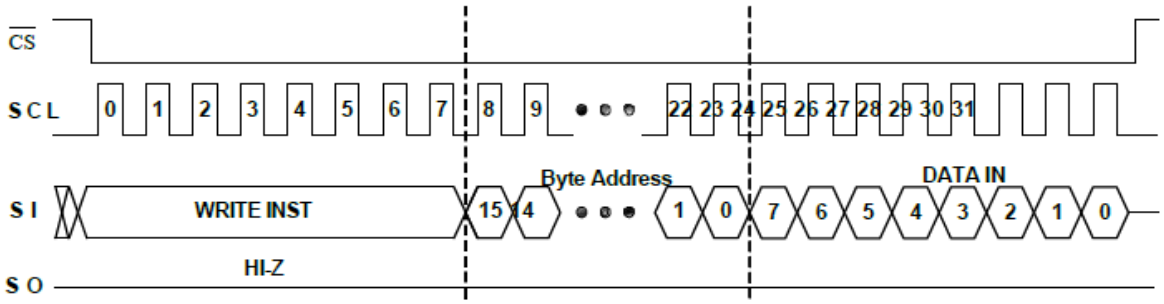


Figure 8: WRITE Timing

Ac Characteristics

Applicable over recommended operating range from: T_{AI} =-40℃ to 85℃，V_{CC} = As Specified,

C_L= 1 TTL Gate and 30 pF (unless otherwise noted) Symbol	Parameter	1.8V~2.7V		2.7V~4.5V		4.5V~5.5V		Units
		Min	Max	Min	Max	Min	Max	
f_{SCK}	Clock frequency, SCK		5		10		20	MHz
t_{RI}	Input Rise Time		2		2		2	μs
t_{FI}	Input Fall Time		2		2		2	μs
t_{WH}	SCK High Time	80		40		20		ns
t_{WL}	SCK Low Time	80		40		20		ns
t_{CS}	$\overline{CS}$ High Time	100		50		25		ns
t_{CSS}	$\overline{CS}$ Setup Time	100		50		25		ns
t_{CSH}	$\overline{CS}$ Hold Time	100		50		25		ns
t_{SU}	Data In Setup Time	20		10		5		ns
t_H	Data In Hold Time	20		10		5		ns
t_{HD}	$\overline{HOLD}$ Setup Time	20		10		5		ns
t_{CD}	$\overline{HOLD}$ Hold Time	20		10		5		ns
t_V	Output Valid	0	80	0	40	0	20	ns
t_{HO}	Output Hold Time	0		0		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z	0	100	0	50	0	25	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z		200		80		40	ns
t_{DIS}	Output Disable Time		200		80		40	ns
t_{WC}	Write Cycle Time		5		5		5	ms

DC Characteristics

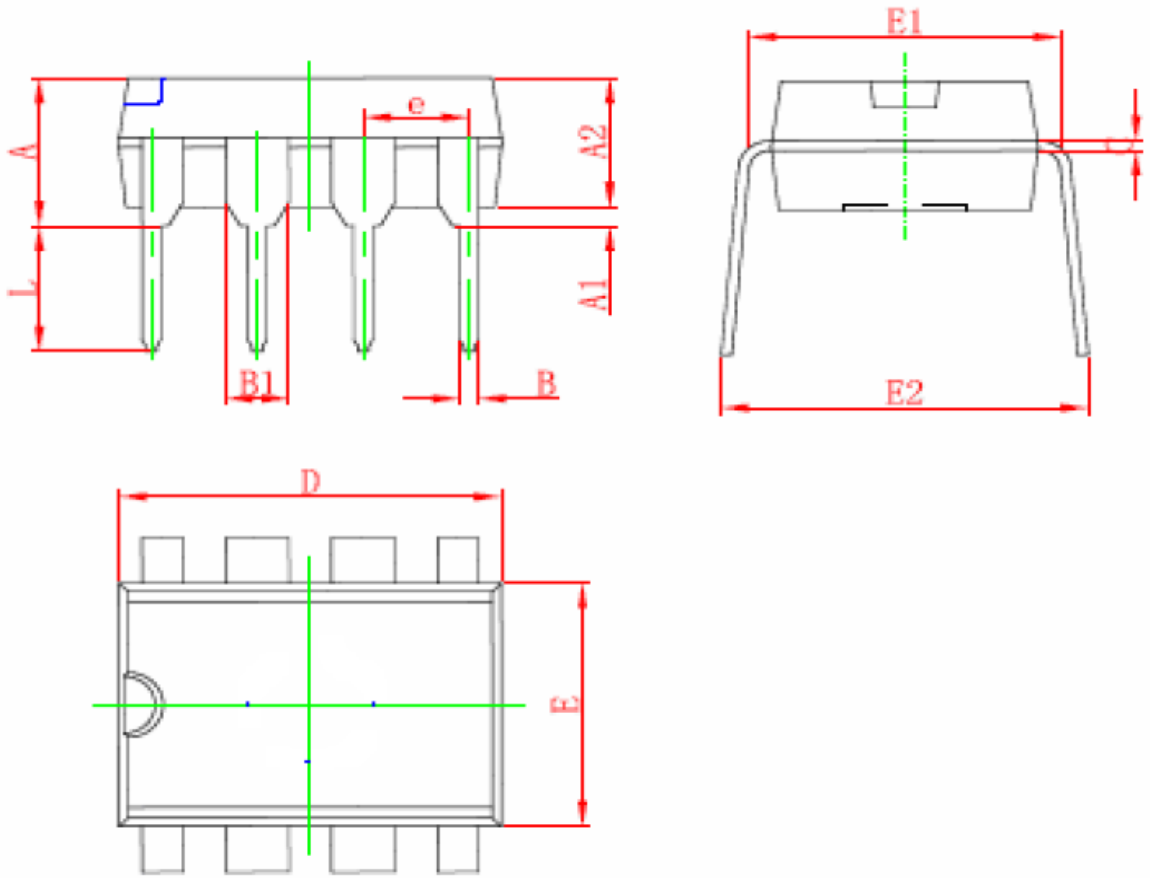
Applicable over recommended operating range from:T_{AI} =-40℃ to 85℃，V_{CC} = 1.8V to 5.5V(unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.7		5.5	V
V_{CC3}	Supply Voltage		4.5		5.5	V
I_{CC1}	Supply Current	V_{CC}=5.0V @ 20MHz, SO=Open,Read		7.5	10.0	mA
I_{CC2}	Supply Current	V_{CC}=5.0V @ 20MHz, SO=Open,Write		4.0	10.0	mA
I_{CC3}	Supply Current	V_{CC}=5.0V @ 5MHz, SO=Open,Read, Write		4.0	6.0	mA
I_{SB1}	Standby current	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}			1.0	μA
I_{SB2}	Standby current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}			1.0	μA
I_{SB3}	Standby current	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}		0.07	1.0	μA
I_{IL}	Input leakage	VIN = VCC or VSS			3.0	μA
I_{OL}	Output leakage	VIN = VCC or VSS			3.0	μA
$V_{IL\ (1)}$	Input low level		-0.6		V_{CC}*0.3	V
$V_{IH(1)}$	Input high level		V_{CC}*0.7		V_{CC}+0.5	V
V_{OL1}	Output low level	3.6V≤V_{CC}≤5.5V, I_{OL} = 3.0mA			0.4	V
V_{OH1}	Output High level	3.6V≤V_{CC}≤5.5V, I_{OH} =-1.6mA	V_{CC}-0.8			
V_{OL2}	Output low level	1.8V≤V_{CC}≤3.6V, I_{OL} = 0.15mA			0.2	V
V_{OH2}	Output High level	1.8V≤V_{CC}≤3.6V, I_{OH} =-100uA	V_{CC}-0.2			

Notes:1. V_{IL} min and V_{IH} max are reference only and are not tested.

Packaging information

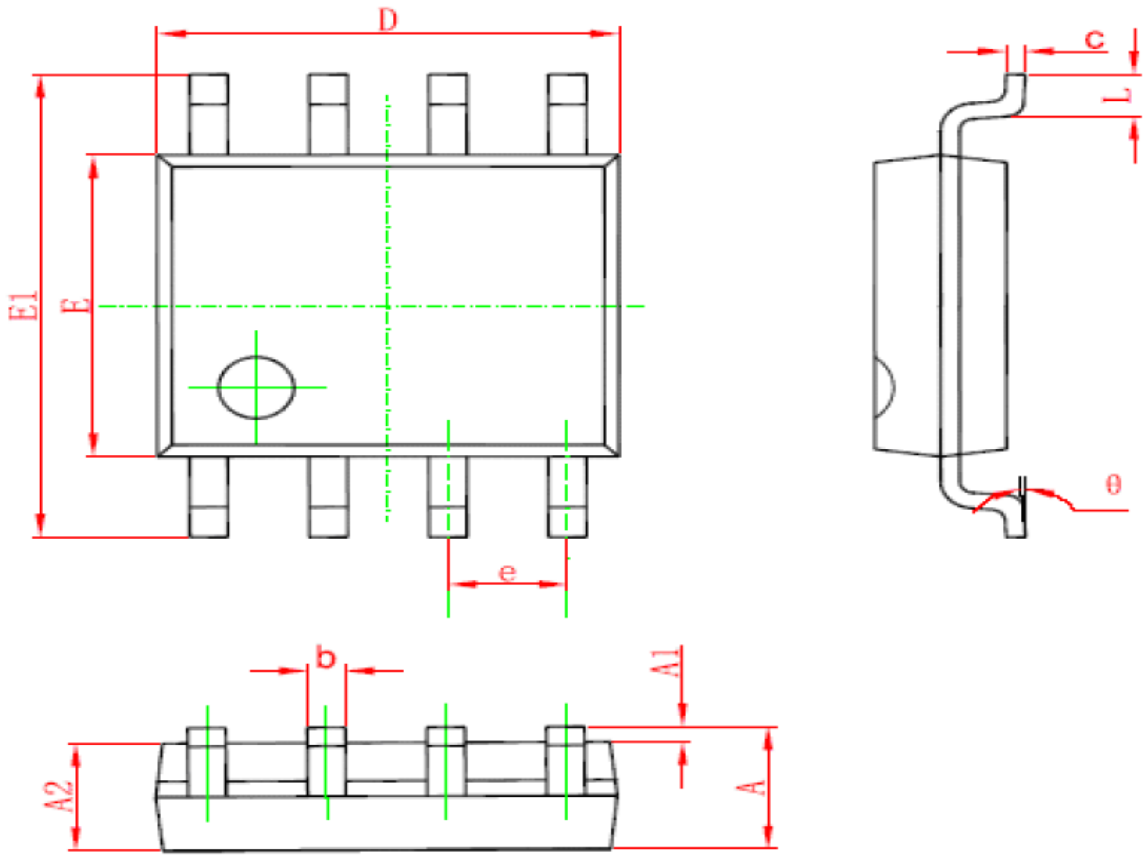
DIP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524（BSC）		0.060（BSC）	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100（BSC）	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

Packaging information

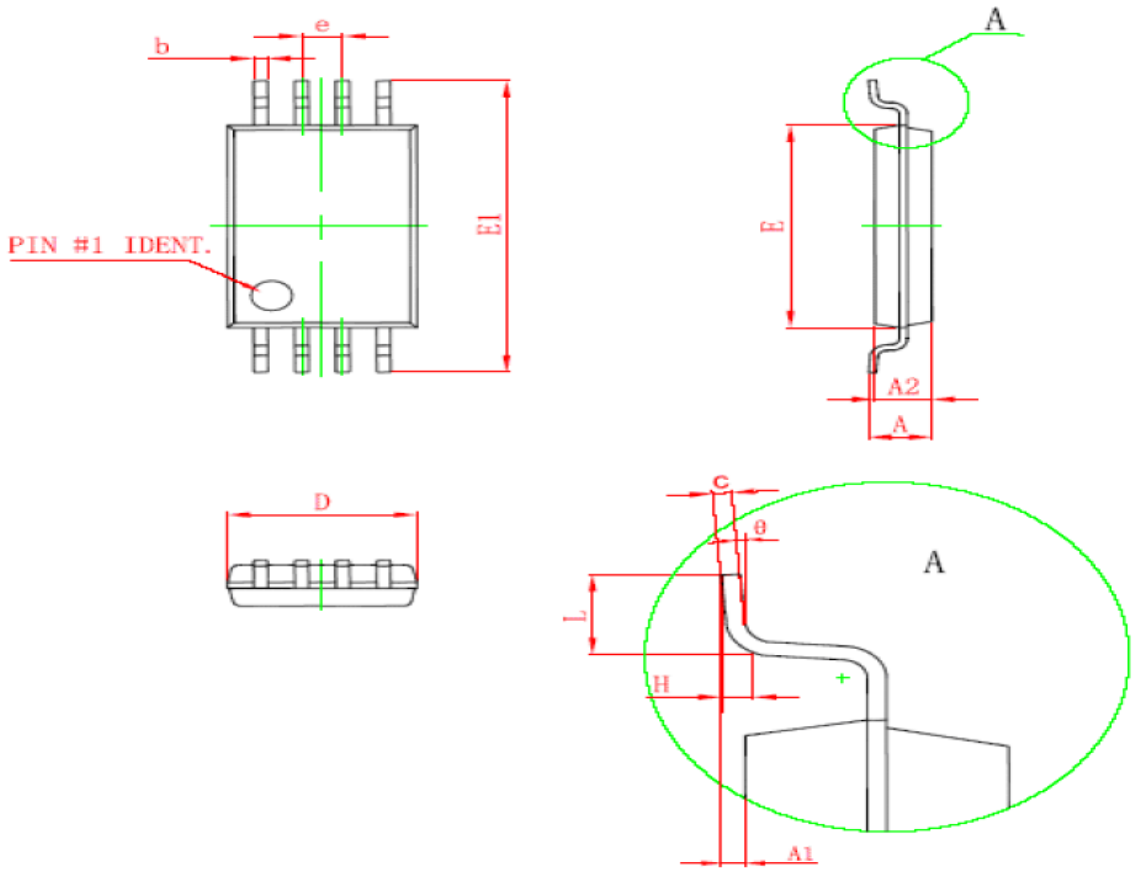
SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Packaging information

TSSOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°

Notes

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and shoes failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.